CLAIMS:

Claims 6, 12 and 20 are canceled, and claims 1, 3-5, 7, 8, 10, 11, 13 and 15-19 are amended herein in the present office action response.

Currently pending claims 1-20 for consideration by the Examiner are as follows:

1. (Currently Amended) A method of forming a bond pad for use in a wirebond interconnection, comprising:

depositing a first layer of bond pad material on a substrate; ~~and~~

depositing a second layer of bond pad material on the first layer, wherein the first layer has a higher ~~Young"s Modulous~~ Young's Modulus of Elasticity than the second layer;

depositing a non-conductive layer over a surface of the second layer of bond pad material;

forming an opening within the non-conductive layer down to the second layer of bond pad material; and

forming a wirebond interconnection within the opening within the non-conductive layer.

2. (Original) The method of claim 1, wherein the first layer comprises a material selected from the group consisting of: $TiAl_x$, an aluminum alloy having at least 2% titanium, an aluminum alloy having at least 2% copper, an aluminum alloy having at least 2% silicon, and an aluminum alloy having at least 2% tungsten; and the second layer comprises of a material selected from the group consisting of: aluminum, aluminum-copper alloys, and aluminum-

titanium alloys.

3. (Currently Amended) The method of claim 1, wherein the ~~Young"s Modulous~~ Young's Modulus of Elasticity of the second layer is less than about 90 GPa, and the ~~Young"s Modulous~~ Young's Modulus of Elasticity of the first layer is at least about 100 GPa or greater.

4. (Currently Amended) The method of claim 1, wherein the first layer of ~~the~~ bond pad material is more resistant to penetration by a probe tip during probe testing than the second layer of ~~the~~ bond pad material.

5. (Currently Amended) The method of claim 1, wherein the first layer of ~~the~~ bond pad material is more resistant to mechanical failure than the second layer of ~~the~~ bond pad material during mechanical testing of ~~a~~ the wirebond interconnection ~~formed on the bond pad~~.

6. (Canceled) The method of claim 1, further comprising:

forming a wirebond interconnection on the bond pad.

7. (Currently Amended) A method of forming a bond pad for use in a wirebond interconnection, comprising:

depositing a first layer of bond pad material on a substrate; ~~and~~

depositing a second layer of bond pad material on the first layer, wherein a hardness of

the first layer is greater than a hardness of the second layer;

forming a wirebond interconnection in mechanical and electrical connection with the second layer.

8. (Currently Amended) The method of claim 7, wherein the hardness of the first layer is about 0.8 GPa and the hardness of the second layer is about 0.6 GPa.

9. (Original) The method of claim 7, wherein the first layer comprises a material selected from the group consisting of: $TiAl_x$, an aluminum alloy having at least 2% titanium, an aluminum alloy having at least 2% copper, an aluminum alloy having at least 2% silicon, and an aluminum alloy having at least 2% tungsten; and the second layer comprises of a material selected from the group consisting of: aluminum, aluminum-copper alloys, and aluminum-titanium alloys.

10. (Currently Amended) The method of claim 7, wherein the first layer of ~~the~~ bond pad material is more resistant to penetration by a probe tip during probe testing than the second layer of ~~the~~ bond pad material.

11. (Currently Amended) The method of claim 7, wherein the first layer of ~~the~~ bond pad material is more resistant to mechanical failure than the second layer of ~~the~~ bond pad material during mechanical testing of ~~a~~ the wirebond interconnection ~~formed on the bond pad~~.

12. (Canceled) The method of claim 7, further comprising:

forming a wirebond interconnection on the bond pad.

13. (Currently Amended) A semiconductor device, comprising:

a first layer formed on a substrate; ~~and~~

a second layer on the first layer, wherein the first layer ~~of the bond pad~~ has a higher ~~Young's Modulous~~ Young's Modulus of Elasticity than the second layer;

a non-conductive layer on the second layer having an opening within the non-conductive layer down to the second layer; and

a wirebond interconnection within the opening within the non-conductive layer forming an electrical connection with the second layer.

14. (Original) The semiconductor device of claim 13, wherein the first layer comprises a material selected from the group consisting of: $TiAl_x$, an aluminum alloy having at least 2% titanium, an aluminum alloy having at least 2% copper, an aluminum alloy having at least 2% silicon, and an aluminum alloy having at least 2% tungsten; and the second layer comprises of a material selected from the group consisting of: aluminum, aluminum-copper alloys, and aluminum-titanium alloys.

15. (Currently Amended) The semiconductor device of claim 13, wherein the first layer ~~of the bond pad~~ is more resistant to mechanical failure than the second layer ~~of the bond pad~~ during mechanical testing of ~~a~~ the wirebond interconnection ~~formed on the bond pad~~.

16. (Currently Amended) The semiconductor device of claim 13, wherein the first layer ~~of the bond pad~~ is more resistant to penetration by a probe tip during probe testing than the second layer ~~of the bond pad~~.

17. (Currently Amended) The semiconductor device of claim 13, wherein the ~~Young"s Modulous~~ Young's Modulus of Elasticity of the second layer is less than about 90 GPa, and the ~~Young"s Modulous~~ Young's Modulus of Elasticity of the first layer is at least about 100 GPa or greater.

18. (Currently Amended) The semiconductor device of claim 13, wherein the hardness of the first layer is about 0.8 GPa and the hardness of the second layer is about 0.6 GPa.

19. (Currently Amended) The semiconductor device of claim 13, ~~further comprising:~~

wherein the non-conductive layer comprises an oxide layer ~~over a surface of the substrate; and~~

~~a via formed within the oxide layer within which the first and second layers of the bond pad are formed~~.

20. (Canceled) The semiconductor device of claim 13, wherein a wirebond interconnection is formed in electrical connection with the bond pad.